REMARKS

Claims 37-48, 61, and 62 are pending, with claims 37, 61, and 62 being independent. Claims 37 and 61 have been amended and claim 62 has been added. Support for the amendments and the new claim can be found in the specification, at least at page 37, line 21 to page 40, line 6 and Fig. 12B. No new matter has been added.

Claims 37-44, 46-48, and 61 have been rejected as being unpatentable over U.S. Patent No. 5,821,138 (Yamazaki '138) or JP 08-288522 (Yamazaki '522) in view of JP 08-293598 (Yoshikazu). Applicant requests withdrawal of this rejection because none of the cited references describes or suggests forming an impurity region that is substantially in parallel with a grain boundary in a crystalline semiconductor film formed over an insulating layer, as recited in claim 37, and forming a pinning region that is substantially in parallel with a grain boundary in a crystallized semiconductor film that is on an insulating surface, as recited in claim 61.

Yamazaki '138 relates to a method of manufacturing a semiconductor device in which a peel-off layer is formed on a quartz substrate 301 and a silicon oxide film 303 is formed on a surface of the peel-off layer 302. See Yamazaki '138 at col. 15, lines 45-65 and Fig. 11A. An amorphous silicon film 304 is formed, a nickel acetate solution is applied on the surface of the film 304 to form a nickel layer 305, and a heat treatment is conducted to crystallize the silicon film 304 and to obtain a crystalline silicon film 306. See Yamazaki '138 at col. 16, lines 12-64 and Figs. 11B and 11C. A thermal oxide film 307 is formed from another heating treatment and the thermal oxide film 307 is removed through etching to obtain a crystalline silicon film 308 that can be etched to form an active layer 309 of a thin film transistor. See Yamazaki '138 at col. 16, line 64 to col. 18, line 34. As the Examiner agrees, Yamazaki '138 fails to describe or suggest forming an impurity region or a pinning region that extends from source and drain regions of the thin film transistor.

Yamazaki '522 relates to a process of making a liquid crystal display that includes forming an amorphous silicon film 104 on an insulating layer 103 and heat-treating to obtain a crystalline silicon film 107. See Yamazaki '522 at paragraphs 0014-0016 and Figs. 1A-D. The crystalline silicon film 107 is made into a barrier layer to form a thin film transistor. See

Yamazaki '522 at paragraph 0016 and Fig. 2A. As the Examiner agrees, Yamazaki '522 fails to describe or suggest forming an impurity region or a pinning region that extends from source to drain regions of the thin film transistor.

Yoshikazu does not remedy the failures of Yamazaki '138 and Yamazaki '522 to describe or suggest this subject matter. Yoshikazu relates to a process for forming an NMOSFET on a surface of a substrate 1. See Yoshikazu at abstract and Fig. 2. The NMOSFET includes a source region 4A and a drain region 4B isolated at a channel region and a plurality of divided channel impurity regions 7 are provided on the channel region of the surface of the substrate 1 between the regions 4A and 4B. See Yoshikazu at abstract and Fig. 2. However, Yoshikazu never describes or suggests that the impurity region 7 is substantially in parallel with a grain boundary in a crystalline semiconductor film formed over an insulating layer or in a crystallized semiconductor film that is on an insulating surface. Rather, Yoshikazu merely explains that a "plurality of divided channel impurity regions 7 are provided in a dotlike plane manner on the channel region of the surface of the substrate 1" without any discussion of the placement of the impurity region 7 relative to a grain boundary. See Yoshikazu at abstract, paragraphs 0031-0035 and Fig. 2.

For at least these reasons, claims 37 and 61 are allowable over any proper combination of Yamazaki '138, Yamazaki '522, and Yoshikazu, as are dependent claims 38-44 and 46-48.

Claim 45 has been rejected as being unpatentable over Yamazaki '138 or Yamazaki '522 in view of Yoshikazu and U.S. Patent No. 5,843,811 (Singh). Claim 45 depends from claim 37, which was rejected as being unpatentable over Yamazaki '138 or Yamazaki '522 in view of Yoshikazu. As discussed above, neither Yamazaki '138, Yamazaki '522, nor Yoshikazu describes or suggests forming an impurity region that is substantially in parallel with a grain boundary in a crystalline semiconductor film formed over an insulating layer, as recited in claim 37. Singh does not remedy the failure of these references to describe or suggest this subject matter. In Singh, a crystalline thin film is fabricated from an amorphous thin film which has been deposited onto a backing substrate. See Singh at col. 2, line 44 to col. 3, line 17. However, Singh never describes or suggests that an impurity region is formed that is substantially in parallel with a grain boundary in the crystalline thin film. Accordingly, claim 37 is allowable

over any proper combination of Yamazaki '138, Yamazaki '522, Yoshikazu, and Singh, as is dependent claim 45.

New claim 62 recites a method of manufacturing a semiconductor device. A crystalline semiconductor film is formed over an insulating surface, a first impurity is added into a portion of the crystalline semiconductor film to form a pinning region, and a second impurity is added into the crystalline semiconductor film to form a source region and a drain region. The pinning region extends between the source region and the drain region and at least two channel regions are separated from each other by the pinning region. The pinning region is substantially in parallel with a grain boundary in the crystalline semiconductor film.

As discussed above, neither Yamazaki '138, Yamazaki '522, Yoshikazu, nor Singh describes or suggests a pinning region that is substantially in parallel with a grain boundary in a crystalline semiconductor film, as recited in claim 62. Accordingly, claim 62 is allowable over the cited art.

The fee in the amount of $120 in payment for a one-month extension of time is being paid concurrently herewith on the Electronic Filing System (EFS) by way of Deposit Account authorization. Please apply any other charges or credits to Deposit Account No. 06 1050.

Respectfully submitted,

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